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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/740,011	12/20/2000	Kazuyoshi Serizawa	NIT-245	4264

24956 7590 12/03/2004

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EXAMINER	
NGUYEN, QUANG N	

ART UNIT	PAPER NUMBER
2141	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/740,011	SERIZAWA ET AL.	
	Examiner	Art Unit	
	Quang N. Nguyen	2141	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Amendment filed on 09/24/2004. Claims 1 and 4-15 have been amended. Claims 1-15 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-15 are rejected under 35 U.S.C. 102(e) as being anticipated by Beardsley et al. (US 6,304,980), herein after referred as Beardsley.

4. As to claim 1, Beardsley teaches a computer system as illustrated in Fig. 2, comprising:

a first storage area for storing data records *(primary DASD 206)* (C9: L14-23);

a first processor *(primary processor 201)* for storing data record to said first storage area asynchronously with said second computer node with the free time interval (C8:L55 - C9:L20);

a transmitter for sending the data records stored in said first storage area *(i.e., a primary storage controller 205 transferring record updates via a primary data mover 204)* (C9: L20-23 and C9: L63 - C10:L13);

a second storage area for storing the data records copied from said first storage area *(secondary DASDs 216)* (C9: L38-43);

a receiver for requesting said transmitter to send the data records stored in said first storage area, receiving the data records from said transmitter and storing the data records to said second storage area *(multiple secondary storage controllers 215 connected to multiple secondary DASDs 216)* (C9: L38-43); and

a second processor *(secondary processor 211)* for designating a record group, which includes at least a part of the data records, to be read from said first storage area in a free time interval asynchronously with said first processor *(i.e., the primary processor 201 transfers data and control information to the secondary processor 211 by*

a communications protocol, for example, a virtual telecommunications access method VTAM communication link 208) and for letting said receiver send a request to said transmitter, wherein said transmitter reads the record group designated by said request sent from said receiver and sends the record group to said receiver *(i.e., the asynchronous data system 200 encompasses collecting control data from the primary storage controllers 205 so that an order of all data writes to the primary DASDs 206 is preserved and applied to the secondary DASDs 216)* (Beardsley, Fig. 2 and C9:L20 – C10:L13).

5. As to claim 2, Beardsley teaches the system of claim 1, wherein said first storage area is allocated within said first computer node *(i.e., within primary site 221 of Fig. 2).*

6. As to claim 3, Beardsley teaches the system of claim 1, wherein said second storage area is allocated within said second computer node *(i.e., within secondary site 231 of Fig. 2).*

7. As to claim 4, Beardsley teaches the system of claim 1, wherein first storage area is allocated within an external storage device connecting with said first computer node and said second computer node *(i.e., wherein a DASD is an external storage device)* (Beardsley, C7: L64-67 and C8: L1-10).

8. As to claim 5, Beardsley teaches the system of claim 1, wherein said second computer node is provided with a timer for starting said second processor with a constant time interval to read the data records to said second storage area from said first storage area *(i.e., wherein in primary node is similar to secondary node)* (Beardsley, C8: L56-67 and C9: L1-14).

9. As to claim 6, Beardsley teaches the system of claim 1, wherein said first processor stores said data records to said first storage area by giving an identifier number indicating the sequence of storing of said data records, said first storage area includes a plurality of entries to store the set of said identifier number and the data records to read the data records from said entry in the inverse direction to the direction to write the data records to said entry with said first processor, and said second processor refers to the data records in said first storage area copied to said second storage area in order to determine whether the relevant data records are correct or not depending on said identifier number (Beardsley, C13: L54-67 and C1: L1-42).

10. As to claim 7, Beardsley teaches the system of claim 6, wherein said first processor writes the identifier number of the relevant data records after having written said data records and said second processor determines that the relevant data records are correct when said identifier number of the data read to said second storage area has continuity but the relevant data records are incorrect when said identifier number does not have continuity (Beardsley, C14: L23-42).

11. As to claim 8, Beardsley teaches the system of claim 1, wherein said first processor further includes an error checking code generator for generating an error checking code for said data record to write said data record and said error checking code to said first storage area and said second processor checks an error, with said error checking code, of the data records read to said second storage area and determines that the relevant data records are correct when no error is checked or incorrect when an error is checked *(i.e., wherein a switch occurs as a result of an error on the primary device, and furthermore if the error occurs on the secondary device the control goes back to the primary device and therefore causing a permanent error)* (Beardsley, C20: L1-29).

12. As to claim 9, Beardsley teaches the system of claim 8, wherein said first storage area includes a plurality of entries for storing a set of said error checking code and the data records to read the data records in the inverse direction to the direction to write the data records to said entry with said first processor (Beardsley, C17: L20-39).

13. Claim 10 is a corresponding system claim of system claim 1, with the addition of wherein transmitting of the data record in said first storage area to said second computer node is performed without intervention of said first and second computer nodes once the transmitting has been started *(Beardsley teaches data transfer is initialized by the microprocessor 410 in the storage path 401 of the storage controller*

205/215 and then once started is controlled by the ADT circuit 415 without microprocessor intervention until completion) (Beardsley, C11: L62-65).

14. As to claim 11, Beardsley teaches a data transfer method comprising:

storing the data record to said first storage area in a desired time interval during operation on said first computer node (Beardsley, C8: L56-67 and C9: L1-13); and

referring to the designated data, through the copying in said second storage area, of said first storage area using said communication means in a desired time interval during operation on said second computer node (Beardsley, C9: L13-37).

15. As to claim 12, Beardsley teaches a data transfer method comprising:

storing the data formed of one or more records in said second storage area using said communication means in a desired time interval during operation on said first computer node (Beardsley, C8: L56-67 and C9: L1-13); and

referring to said data in the second area in a desired time interval during operation on said second computer node, (Beardsley, C9: L13-37).

16. As to claim 13, Beardsley teaches a data transfer method comprising:

a first step for storing data formed of one or more records to said first storage area in a desired time interval using said first communication means during operation on said first computer node (Beardsley, C8: L56-67 and C9: L1-13); and

a second step for referring to the designated data in said first storage area by copying such data to said second storage area using said second communication means in a desired time interval asynchronously with said first step during operation on said second computer node (Beardsley, C9: L13-37).

17. As to claim 14, Beardsley teaches the method of claim 11, further comprising:

a step in which said first storage area includes a plurality of entries wherein a set of identifier number and data record is stored, operates on said first computer node, writes said identifier number of the relevant data record after writing said data record and then reads said data record from said entry in the inverse direction to the direction to write data record to said entry (Beardsley, C13: L54-67); and

a step for referring to the data in said first storage area copied to said second storage area and determining that relevant data record is correct when said identifier number of the data read to said second storage area has continuity or incorrect when said identifier number does not have continuity during operation on said second computer node (Beardsley, C14: L1-35).

18. As to claim 15, Beardsley teaches the method of claim 11, further comprising:

a step in which said first storage area includes a plurality of entries to which a set of the error checking code and data record is stored *(i.e., stored in maintenance log)*, operates on said first computer node, writes said data record and its error checking

code to said first storage area and reads the data record from said entry in the direction identical to the direction to write data record to said entry (Beardsley, C17: L20-39); and

a step for checking an error with said error checking code for the data read to said second storage area and determines that relevant data record is correct when no error is detected or is incorrect when an error is checked during operation on said second computer node (Beardsley, C14: L14-42).

Response to Arguments

19. In the remarks, applicant argued in substance that

(**A**) Prior Art does not teach or suggest "a receiver in one of the computers requests a transmitter in the other computer to transfer data records stored in the main storage in the other computer", as claimed in claim 1.

As to point (**A**), Beardsley teaches the storage controller *(i.e., one of the secondary storage controllers 215)* contains four storage paths 401 connected to an 8x2 switch 402 by an upper channel port 430 and to a plurality of DASDs 216 by a lower device port 432, wherein the storage path 401 directs the transfer of data records (Beardsley, C11: L20-33). In addition to directing the transfer of data, the storage path 401 also maintains the status of one or more duplex pairs and sets/resets flags within

the control blocks to indicate when the secondary DASD 107 needs to be synchronized with the primary DASD 104 *(i.e., requesting to transfer data from one computer to another)* (Beardsley, C12: L31-62).

(**B**) Prior Art does not teach or suggest of "performing transferring, copying or storing of data records without intervention of the processors in the computer system, other than the processor in the coupled communication means, once the transferring or copying or storing has been started", as claimed in claims 11, 12 and 13.

As to point (**B**), in response to applicant's arguments, the recitation in the quotations "performing transferring, copying or storing of data records without intervention of the processors in the computer system, other than the processor in the coupled communication means, once the transferring or copying or storing has been started" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

20. Applicant's arguments as well as request for reconsideration filed on 09/24/2004 have been fully considered but they are not deemed to be persuasive.

21. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang N. Nguyen whose telephone number is (571) 272-3886.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's SPE, Rupal Dharia, can be reached at (571) 272-3880. The fax phone number for the organization is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RUPAL DHARIA
SUPERVISORY PATENT EXAMINER